

Claims

1-20 (canceled)

21. (New) A system, comprising:

a random access memory device;

a first signal line coupled to the random access memory device, the first signal line to carry a first signal;

a second signal line coupled to the random access memory device, the second signal line to carry a second signal; and

a memory controller coupled to the first signal line and the second signal line, wherein the memory controller includes a delay locked loop to generate the first signal, wherein the first signal is used to transmit data to the random access memory device, the delay locked loop to receive the second signal such that the second signal is used to sample read data provided by the memory device.

22. (New) The system as recited in claim 21, wherein the memory controller includes a driver such that the first signal is used to transmit data to the memory device by way of the driver.

23. (New) The system as recited in 21, wherein the memory controller includes a sampler to sample the read data using the second signal.

24. (New) The system as recited in claim 21, further comprising:

a first delay element coupled in a feedback path of the delay-locked loop to change a phase difference between the second signal and a reference clock signal by a first time period.

25. (New) The system as recited in claim 24, further comprising:  
a second delay element outside the feedback path of the delay-locked loop  
to receive the second signal, and  
to delay the first signal relative to the second signal by the first time  
period.

26. (New) The system of claim 21, further including a clock generator to generate the second signal, wherein the second signal propagates from the clock generator to the memory controller.

27. (New) The system of claim 26, wherein the second signal is terminated after being received by the memory controller.

28. (New) The system of claim 21, wherein the first signal is a clock signal and the second signal is a clock signal.

29. (New) The system as recited in claim 21, wherein the delay-locked loop further includes a phase detector to identify phase differences between the second signal and the reference clock signal.

1 30. (New) The system as recited in claim 29, wherein the phase detector  
2 is a zero phase detector.

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4 31. (New) The system as recited in claim 29, wherein the phase detector  
5 is an integration sampler to integrate the first signal with respect to the reference  
6 clock signal.

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8 32. (New) The system as recited in claim 21, wherein the delay-locked  
9 loop further includes a 180 degree phase shift circuit to adjust a phase of the  
10 second signal..

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12 33. (New) The system as recited in claim 32, wherein the 180 degree  
13 phase shift is accomplished by switching over the first signal line and the second  
14 signal line.

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16 34. (New) The system as recited in claim 21, wherein first data of the  
17 read data is sampled on a rising edge of the second signal and second data of the  
18 read data is sampled on a falling edge of the second signal.

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20 35. (New) The system as recited in claim 21, wherein the delay lock loop  
21 generates a receive clock using the second signal, wherein the receive clock is used  
22 to sample read data by way of the second signal.



1 41. (New) The method as recited in claim 40, further comprising  
2 delaying the first signal relative to the second signal by the first time period.

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4 42. (New) The method of claim 37, further comprising generating the  
5 second signal from a clock generator and propagating the second signal to a  
6 memory controller.

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8 43. (New) The method of claim 42, further comprising terminating the  
9 second signal after the second signal is received by the memory controller.

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11 44. (New) The method of claim 37, wherein the first signal is a clock  
12 signal and the second signal is a clock signal.

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14 45. (New) The method as recited in claim 37, further comprising  
15 identifying phase differences between the second signal and the reference clock  
16 signal.

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18 46. (New) The method as recited in claim 45, further comprising  
19 detecting a zero phase difference.

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21 47. (New) The method as recited in claim 45, further comprising  
22 integrating the first signal with respect to the reference clock signal.

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24 48. (New) The method as recited in claim 37, further comprising  
25 adjusting a phase of the second signal by 180 degrees.

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2 49. (New) The method as recited in claim 48, further comprising  
3 switching over the first signal line and the second signal line to effect the 180  
4 degree phase shift.

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6 50. (New) The method as recited in claim 37, wherein first data of the  
7 read data is sampled on a rising edge of the second signal and second data of the  
8 read data is sampled on a falling edge of the second signal.

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10 51. (New) The method as recited in claim 37, further comprising  
11 generating a receive clock using the second signal, wherein the receive clock is  
12 used to sample read data by way of the second signal.

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14 52. (New) The method of claim 51, further comprising generating the  
15 receive clock such that a phase of the receive clock is aligned with a phase of the  
16 second signal.

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18 53. (New) A system, comprising:  
19 an electronic data store;  
20 a controller for the electronic data store, including:  
21 a delay-locked loop to receive a second signal, wherein the delay-  
22 locked loop includes:  
23 a first delay element coupled in a feedback path of the delay-  
24 locked loop, wherein the first delay element changes a phase difference between  
25 the second signal and a reference clock signal by a first time period, and

1 a second delay element outside the feedback path to receive  
2 the second signal and output a first signal that is delayed relative to the second  
3 signal by the first time period; and

4 a phase detector to determine phase differences between the second  
5 signal and the reference clock signal.

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7 54. (New) The system as recited in claim 53, wherein the phase detector  
8 comprises a zero phase detector.

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10 55. (New) The system as recited in claim 53, wherein the delay-locked  
11 loop further includes a 180 degrees phase shifter.

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13 56. (New) The system as recited in claim 53, wherein the first and  
14 second signals provide timing for address multiplexing operations of the electronic  
15 data store.

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17 57. (New) The system as recited in claim 53, further comprising an  
18 integration sampler to integrate the first signal with respect to the reference clock  
19 signal.

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21 58. (New) A system, comprising:  
22 means for electronic storage of data; and  
23 means for controlling the electronic storage of data, including:  
24 means for generating a first signal and a second signal, the means for  
25 generating including:

1 a first means for delaying data transfer of the second signal to  
2 be used for changing a phase difference between the second signal and a reference  
3 clock signal by a first time period, and

4 a second means for delaying data transfer of the first signal to  
5 be used for receiving the second signal and outputting the first signal that is  
6 delayed relative to the second signal by the first time period.  
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